REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Claim Rejections - 35 USC § 103

Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tzannes et al U.S. Patent No 5,636,246 in view of Trelewicz U.S. Patent No 5,774,751. Applicants respectfully traverse these rejections.

There are three basic criteria to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a). First, there must be some suggestion or motivation in the cited references to modify or combine their teachings; second, there must be reasonable expectation of success; and third, the prior art references must teach or suggest all the claim limitations. *See* M.P.E.P §2142. As to claim 1, the combination of cited references does not teach or suggest all the claim limitations.

Citing the clock recovery circuit of Trelewicz, the Examiner has stated that "Trelewicz teaches a loop recovery is the **same as the claimed (backtracking)** (see fig.1 element 36) (see col.2, lines 30-45 over previously decoded portions (see fig.1 element 44 and col.3, lines 6-10) of the transmission" (Emphasis added). Applicants respectfully point to the Examiner that the clock recovery circuit of Trelewicz is actually configured to track errors and symbols and to generate a data rate clock and phase offset for symbol interpolator 34 to interpolate linearly between samples to form each symbol (*see* col. 2, lines 16-32). The clock recovery circuit aids in forming symbols before these symbols are decoded by the symbol decoder 38 (*see* figure 1). Therefore, the clock recovery is not backtracking as recited in claim 1. Claim 1 recites backtracking over previously decoded portions of the transmission, which is actually after the symbols have been decoded, error is detected, and a digital signal processor is reconfigured to decode symbols again with the reconfigured information. Trelewicz does not teach this limitation.

Further, the Examiner has stated that

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> "controller (see figs. 1, 3 elements 131, 324) is the same as the claimed (reconfiguring) a digital signal processor (see fig.1 equalizer 124) to take into account the narrowband interference (see 8, lines 10-16). **Since the controller of Tzannes controls the equalizer**, which is the same as the claimed digital processor, **to adapt to monitor the narrow band interference** therefore the reconfiguration process is taught by Tzannes." (Emphasis added)

Applicants respectfully point to that Examiner that claim 1 recites reconfiguring a digital signal processor to take into account the narrowband interference and decoding the transmission using the reconfigured digital signal processor. In contrast, a careful reading of the cited sections reveal that the receiver controller 304 is configured to detect narrowband interference in the received signal and inform the transmitter controller 304 to stop using bands that experience the narrowband interference (*see* col. 8, lines 15-22). This is completely different than decoding the transmission using the reconfigured digital signal processor as recited in claim 1.

Accordingly, the combination of cited reference does not teach each and every limitation of claim 1 and claim 1 and those dependent therefrom are clearly and patentably distinguishable from the combination of cited references.

Claims 15-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Tzannes et al U.S. Patent No 5,636,246. Applicants respectfully traverse these rejections.

As to the antenna, the Examiner has stated that Tzannes et al. discloses "a receiver for receiving transmissions transmitted over a communications "**medium**" (see fig.1 element 150), therefore the antenna for receiving is inherent taught by Tzannes" (Emphasis added). Applicants respectfully point to the Examiner that Tzannes et al. does not use the term "medium". In fact, it uses the term "communication **link**" and it is clearly shown as element 113 in Figure 1, element 250 in Figure 2, and element 340 in Figure 3. Tzannes et al. further describes connection of subscribers to a central office (*see* col. 2, lines 1-5), which is typically done using communication links as shown and described by Tzannes et al. Therefore, Tzannes et al. does not teach an antenna explicitly or inherently.

As to the sequential decoder, the Examiner has not provided any citation in Tzannes et al. that discloses the sequential decoder as recited in claim 15.

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As to two distinct information and control lines recited in claim 15, the Examiner has cited a single element, the control unit 131, of Tzannes et al. Further, the Examiner has stated that:

> "the controller of Tzannes et al monitors the **recovered symbols for errors**, detects narrowband interference and signals the transmitter to prevent data from being placed in corrupted channel and finally initiates convolution information in a shift register (see col.8, lines 10-15 and col.9, lines 3-8). Since these three steps (monitoring, detecting and initiating) are essential to operation and the configuration of the transceiver of Tzannes, therefore the controller having first and second control lines to provide configuration and operational information is **inherently taught** by Tzannes as to perfectly synchronize the receiver and transmitter as taught by Tzannes (see col.7, lines 13-17). (Emphasis in original and added)

Applicants respectfully point to the Examiner that claim 15 recites a first control and information line providing configuration and operational information of the digital processing unit; and a second control and information line providing configuration and operational information of the sequential decoder.

First, the Examiner has not cited a sequential decoder in Tzannes et al. so the second control and information line cannot be taught by Tzannes et al.

Second, a careful reading of cited sections reveals that actually the controller 131 monitors the "**recovered symbols**" as the Examiner has also noted, which means the output of the decoder 128; however, the Examiner has cited Equalizer 124 as the digital processing unit recited in claim 15. Further, because the controller 131 monitors **recovered symbols** for narrowband interference, determines the bands that include the interference, and informs the controller in the transmitter to skip those bands, the configuration and operational information of the Equalizer 124 does not get affected and not used by the controller 131 and the Examiner has not cited any section in Tzannes et al. that suggests otherwise. Accordingly, Tzannes et al. does not teach each and every limitation of claim 15 and claim 15 and those depend therefrom are patentably distinguishable from the combination of cited references.

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As to claim 16, the Examiner has simply cited the function of the controller 131 (col. 8, lines 10-19), which actually the Examiner has also cited as the first and second control and information lines recited in claim 15. Applicants respectfully point to the Examiner that the cited reference must teach each and every limitation and element recited in the claim. Tzannes et al. does not teach every limitation of claim 16.

As to claim 17, the Examiner has stated that "Tzannes et al **would teach** wherein the interference detection unit is **a Bluetooth transmission detector** as to perfectly synchronization operation the receiver and transmitter." Applicants respectfully point to the Examiner that Tzannes et al. do not even mention Bluetooth in their disclosure. Accordingly, Tzannes et al. do not teach limitations of claim 17.

As to claim 18 and 20, the Examiner has stated that "Tzannes et al. wherein the radio receiver further comprises a **shift register is the same as the claimed (memory)** (see fig.1 element 118 or 122 and col.4, lines 3-5) coupled to the digital processing unit and the sequential decoder, the memory containing **pre-computed profiles of a plurality of different types of interference and errors**."

Applicants respectfully request a careful reading of claim 18 and 20 and cited reference. In the cited sections, Tzannes et al. actually describes a shit register 118 that holds incoming digitized signal and register 122 holds the output of the time to frequency-domain transform. Nowhere in the entire disclosure Tzannes et al. describes pre-computed profiles of a plurality of different types of interference and errors.

As to claims 19, the Examiner has simply repeated the claim and stated that "As per claim 19, Tzannes et al **would teach**, wherein the pre-computed profiles may be loaded into the digital processing unit and the sequential decoder immediately upon detection of interference and errors as to perfectly synchronization operation the receiver and transmitter." Applicants request a careful examination of claim 19 with proper citations. Further, "would teach" is not a proper basis for rejecting a claim and the Examiner has not cited any section in the reference that actually teaches pre-computed profiles as recited in the claim.

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Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trelewicz U.S. Patent No 5,574,751. Applicants respectfully traverse these rejections.

Applicants respectfully point to the Examiner that explained in response to claim 1 rejection Trelewicz does not even discuss backtracking through symbols. Instead, in the cited sections, Trelewicz actually adjusts coefficients for metric calculation. This has nothing to do with backtracking through received symbols as recited in claim 23. Accordingly, claim 23 and those depending therefrom are patentably distinguishable from Trelewicz.

Applicant believes this application and the claims herein to be in a condition for allowance. Please charge any additional fees, or credit overpayment to Deposit Account No. 20-0668. Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,

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